

Understanding of Ferroelectric Material for Capacitors and Transistors of Non-volatile Memory

Fadlioni Fadlioni^{1*}, Priani Gagani Chamdareno¹, Budiyanto Budiyanto¹,
Haris Isyanto¹

¹ Teknik Elektro Universitas Muhammadiyah Jakarta
*fadlioni@ftumj.ac.id

Abstract

Field effect transistors in non-volatile memory use ferroelectric material as a gate insulator. By designing ferroelectric transistors, power dissipation in non-volatile memory can be reduced so they can get devices that can operate with small voltages and produce large currents because by reducing the voltage, the device size can be reduced. Simulation and analysis are very important to achieve this because with simulations and analyzes, time and costs can be reduced and optimal results can be obtained.

Keywords: ferroelectric, field, effect, transistors

1. Introduction

Power dissipation in integrated electronic circuits is very dependent on the voltage needed to switch the field effect transistor to the on or off state [1]. Reducing the operating voltage is needed to reduce power consumption, reduce the dimension of the device and reduce the price per transistor [2], [3]. However, Boltzman's distribution of electrons represents a fundamental low limit of 60 mV per decade at room temperature [4]. The use of ferroelectric differential negative capacitance has been proposed to solve this problem by increasing the gate voltage of a passive field effect transistor [5]. In theory, it is possible to stabilize the state of the ferroelectric negative capacitance as long as the total capacitance of the system is positive through the series connection between the ferroelectric gate insulator and the positive semiconductor capacitance on the transistor [6]. Several cases of increased capacitance in ferroelectric-dielectric hetero structures have been reported so far [7] - [9]. Furthermore, transient negative capacitance has been observed directly on ferroelectric capacitors by applying pulsed voltage to the R-C network by using zirconate titanate (PZT) leads [10]. However, for applications in transistors, HfO₂ thin film ferroelectrics are preferred because they are compatible with semiconductor manufacturing standards and because ferroelectric characters are at least 5 nm thick [11] - [15].

2. Methods and Literature Review

A capacitor is defined as two conductors that can hold opposite charges and the capacitance value will change if the distance and relative position between two conductors change due to external forces [16]. The capacitance value of a capacitor is given by $C = \epsilon_0 \epsilon_r w l / d_0$ where ϵ_0 is the free space permittivity value (8.8546×10^{-12} F/m), relative permittivity, w and l are respectively width and the length of the electrode capacitor and d_0 is the gap between the electrodes [17]. Ferroelectric phenomena are defined as phenomena where a material exhibits a spontaneous and reversible polarization under the influence of an external electric field [18] - [20]. Ferroelectric materials are used in storage capacitors in dynamic random access memory (DRAM) [21], [22]. A ferroelectric field effect transistor is a transistor in which the gate insulator is ferroelectric material. Non-volatile

memory is defined as memory that can maintain its state even though the power supply is turned off [23], [24]. Data analysis in this research is simulation, modeling and literature study. It is important to choose a data set that represents a single cycle of electric field waves which can then be used to construct polarization loops against electric fields. Data points corresponding to the starting and ending points of a loop are identified using a "threshold routine" that detects when the electric field waves across the horizontal time axis with both positive and negative slopes. When the necessary data points have been identified, the charge Q stored by the test sample at the given time t is calculated by numerical integrations from current data I given by equation 1.

$$Q(t) = \int_{t_1}^{t_2} I dt \dots \dots \dots (1)$$

Dielectric displacement D can be calculated by the surface charge density given by equation 2 where A is outside the surface of the test sample.

$$D(t) = \frac{Q(t)}{A} \dots \dots \dots (2)$$

The surface of the test sample can be assumed to be a circle such that

$$A = \pi r^2 \dots \dots \dots (3)$$

In most cases for ferroelectric with high permittivity, the polarization of P at the given time is almost the same as the dielectric displacement D . However, a slight correction is needed to give accurate results for dielectric with low permittivity.

$$D(t) = P(t) - \epsilon_0 E(t) \dots \dots \dots (4)$$

$$P(t) = D(t) - \epsilon_0 E(t) \dots \dots \dots (5)$$

Figure 1(a) shows a cross section of a ferroelectric capacitor in which a ferroelectric material is enclosed in 2 metal thin films. The metal here can be gold (Au), silver (Ag) or other. Figure 1(b) is a 3-dimensional schematic of a ferroelectric capacitor. Here the metal terminal can be circular or square in shape. Figure 1(c) shows a cross section of a semiconductor ferroelectric metal field effect transistor. The metal on the left or right works as a drain or a source terminal while the metal below is the terminal gate. The 3-dimensional schematic of the semiconductor ferroelectric metal field effect transistor is shown in Figure 1(d). Drain current will increase if the distance between the drain terminal and source is reduced.

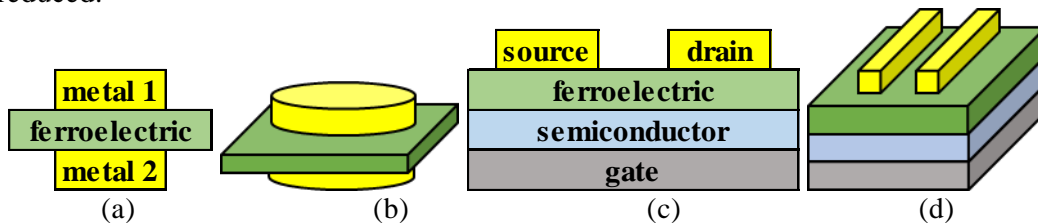


Figure 1 schematic of (a) cross section of ferroelectric capacitors, (b) 3-dimensional ferroelectric capacitors, (c) cross section of a semiconductor ferroelectric metal field effect transistor, (d) 3-dimensional semiconductor ferroelectric metal field effect transistor.

3. Results and Discussion

The development of a simple hysteresis loop model and the determination of factors that influence the shape of hysteresis remain an interesting challenge for theoretical studies. The method of measuring ferroelectric capacitors is shown in Figure 2(a) where the voltage is applied to one metal and the other metal is grounded. Figure 2(b) is a hysteresis curve of a ferroelectric. The horizontal axis can be in voltage or electric field (voltage divided by thickness), while the vertical axis is polarization.

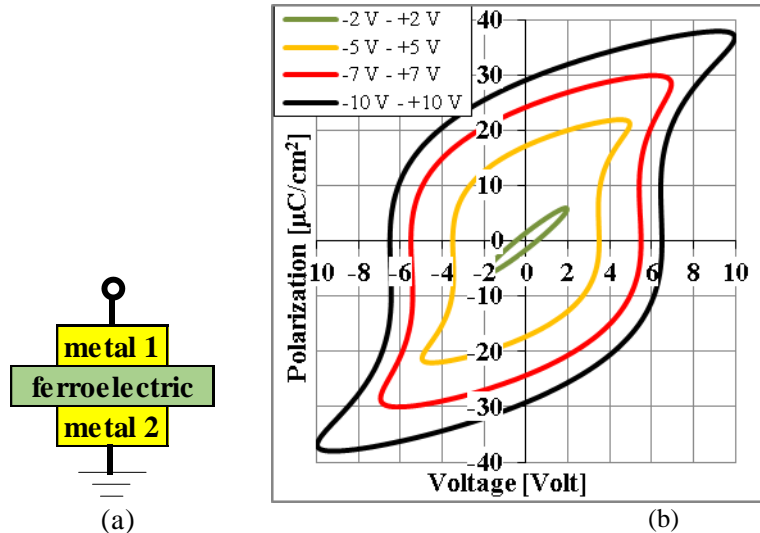


Figure 2(a) schematic measurement of ferroelectric capacitor polarization measurements, (b) polarization versus stress hysteresis curves of ferroelectric material.

Figure 3 shows a schematic measurement of drain current characteristics with respect to the drain voltage with varying V_G . Figure 4(a) is a characteristic of I_D - V_D MOSFET. The flat axis is the drain voltage and the vertical axis is the drain current. Overall, when the gate voltage is positive, the source drain current increases as the drain voltage increases. The increase in drain source current along with the change in gate voltage in the positive direction is due to the increase in the negative electron carrier charge induced by the positive gate voltage. Meanwhile, when the drain voltage becomes more positive, the source drain current increases, but at a current the voltage becomes saturated and does not increase again at a positive drain voltage. Figure 4(b) shows the drain current curve with respect to the drain voltage. When $V_G > V_{TH}$ and $V_D < V_G - V_{TH}$, the transistor comes alive and a channel is formed that allows current to flow between drain and source. At present, the transistor operates like a resistor that is controlled by gate voltage relative to the source and drain voltage. When $V_G > V_{TH}$ and $V_D > V_G - V_T$, the transistor becomes on and channel is formed which allows current to flow between drain and source. Because the drain voltage is greater than the source voltage, electrons spread and conduction does not pass through narrow canals but through a wider 2 or 3 dimensional current distribution. This condition is called pinch-off to indicate the shortage of areas near the drain.

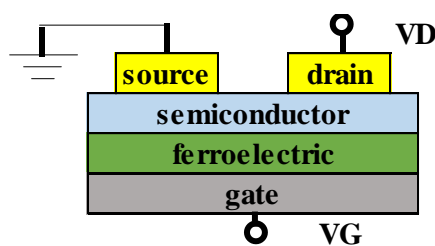


Figure 3 Schematic measurement of drain current to drain voltage with different gate voltages.

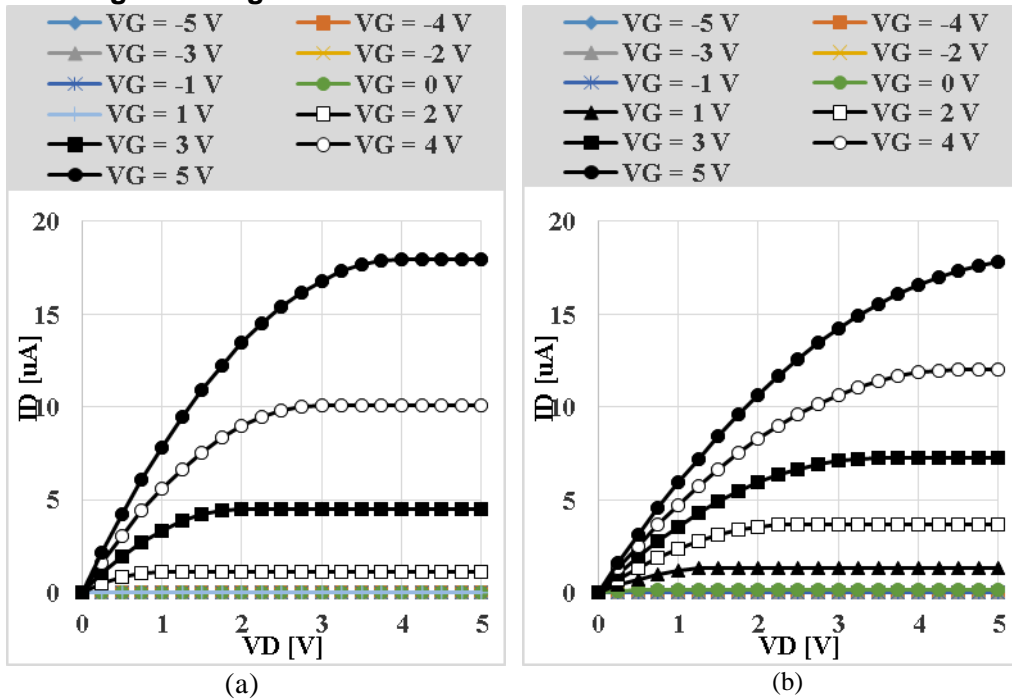


Figure 4 (a) the drain current curves against the drain voltage with the gate are biased from -6 V to +6 V, (b) the drain current curves against the drain voltage with the gate are biased from +6 V to -6 V.

Figure 5(a) shows a schematic measurement of the characteristics of the drain current to the drain voltage with the varied V_G . Figure 5(b) shows the drain current curve with the gate voltage.

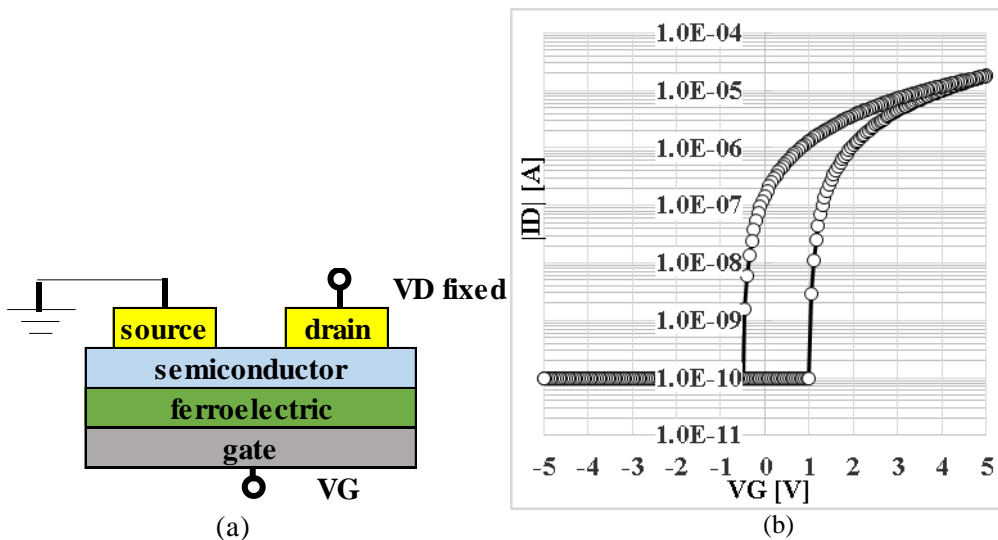


Figure 5 (a) Schematic measurement of drain current to gate voltage, (b) the absolute value curve of the drain current to the gate voltage.

4. Conclusion

Ferroelectric materials are used for gate insulators in field effect transistors that are used for non-volatile memory. Non-volatile memory is memory where data can

be written and deleted, but the data will still be there even in the off condition. The relationship between the results of the simulation with the title is that spontaneous polarization of the ferroelectric material implies a hysteresis effect that can be used as a memory function. From the polarization curve to the voltage and the drain current curve to the gate voltage, it can be concluded that, even when the power is 0 (voltage 0), the current and polarization can still be maintained.

Acknowledgments

This research is partially funded by research grant from LPPM Universitas Muhammadiyah Jakarta 31A/LPPM-UMJ/II/2018, contract number: 46.A/LPPM-UMJ/III/2018 and research grant from Faculty of Engineering Universitas Muhammadiyah Jakarta 56/PAKARTI-FT-UMJ/IX/2019 contract number 368/F.4-UMJ/IX/2019.

References

- [1] E. Pop, "Energy dissipation and transport in nanoscale devices," *Nano Research*, vol. 3, no. 3, pp. 147–169, Mar. 2010.
- [2] R. H. Dennard, F. H. Gaensslen, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion-implanted MOSFET's with very small physical dimensions," *IEEE Journal of Solid-State Circuits*, vol. 9, no. 5, pp. 256–268, 1974.
- [3] G. E. Moore, "Electronics 38, 114 (1965)," *Google Scholar GM Moore, Proc. IEEE*, vol. 86, p. 82, 1998.
- [4] V. V. Zhirnov and R. K. Cavin, "Nanoelectronics: Negative capacitance to the rescue?," *Nature Nanotechnology*, vol. 3, no. 2, p. 77, 2008.
- [5] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," *Nano letters*, vol. 8, no. 2, pp. 405–410, 2008.
- [6] S. Salahuddin and S. Datta, "Can the subthreshold swing in a classical FET be lowered below 60 mV/decade?," in *2008 IEEE International Electron Devices Meeting, 2008*, pp. 1–4.
- [7] A. Islam Khan et al., "Experimental evidence of ferroelectric negative capacitance in nanoscale heterostructures," *Applied Physics Letters*, vol. 99, no. 11, p. 113501, 2011.
- [8] D. J. Appleby et al., "Experimental observation of negative capacitance in ferroelectrics at room temperature," *Nano letters*, vol. 14, no. 7, pp. 3864–3868, 2014.
- [9] W. Gao et al., "Room-temperature negative capacitance in a ferroelectric–dielectric superlattice heterostructure," *Nano letters*, vol. 14, no. 10, pp. 5814–5819, 2014.
- [10] A. I. Khan et al., "Negative capacitance in a ferroelectric capacitor," *Nature materials*, vol. 14, no. 2, p. 182, 2015.
- [11] T. S. Bösecke, J. Müller, D. Bräuhäus, U. Schröder, and U. Böttger, "Ferroelectricity in hafnium oxide thin films," *Applied Physics Letters*, vol. 99, no. 10, p. 102903, 2011.
- [12] J. Müller, P. Polakowski, S. Mueller, and T. Mikolajick, "Ferroelectric hafnium oxide based materials and devices: Assessment of current status and future prospects," *ECS Journal of Solid State Science and Technology*, vol. 4, no. 5, pp. N30–N35, 2015.
- [13] J. Muller et al., "Ferroelectricity in simple binary ZrO₂ and HfO₂," *Nano letters*, vol. 12, no. 8, pp. 4318–4323, 2012.
- [14] M. H. Park et al., "Ferroelectricity and antiferroelectricity of doped thin HfO₂- based films," *Advanced Materials*, vol. 27, no. 11, pp. 1811–1831, 2015.
- [15] M. Hoffmann et al., "Stabilizing the ferroelectric phase in doped hafnium oxide," *Journal of Applied Physics*, vol. 118, no. 7, p. 072006, 2015.
- [16] D. Zhang and B. Wei, "Design and analysis of a collision detector for hybrid robotic machine tools," *Sensors & Transducers*, vol. 193, no. 10, p. 67, 2015.
- [17] S. Cruz, D. Dias, J. C. Viana, and L. A. Rocha, "Inkjet printed pressure sensing platform for postural imbalance monitoring," *IEEE Transactions on Instrumentation and Measurement*, vol. 64, no. 10, pp. 2813–2820, 2015.

- [18] R. E. Newnham and L. E. Cross, "Ferroelectricity: The foundation of a field from form to function," MRS bulletin, vol. 30, no. 11, pp. 845–848, 2005.
- [19] T. Shimada and T. Kitamura, "Multi-physics properties in ferroelectric nanowires and related Structures from first-principles," Nanowires, p. 353, 2010.
- [20] R. Ramesh and N. A. Spaldin, "Multiferroics: progress and prospects in thin films," Nature materials, vol. 6, no. 1, p. 21, 2007.
- [21] B.-E. Park, H. Ishiwara, M. Okuyama, S. Sakai, and S.-M. Yoon, Ferroelectric-Gate Field Effect Transistor Memories. Springer, 2016.
- [22] X. Wang et al., "Two-dimensional negative capacitance transistor with polyvinylidene fluoride-based ferroelectric polymer gating," npj 2D Materials and Applications, vol. 1, no. 1, p. 38, 2017.
- [23] T. Y. H. ERIC, "Non-volatile Polymer Memory for Si IC Applications," 2009.
- [24] G. Sun, "Exploring memory hierarchy design with emerging memory technologies," 2014.